I CLAIM

1. A data processing apparatus comprising:

a processor core operable to process a sequence of instructions, said processor core having a plurality of pipeline stages, one of said plurality of pipeline stages being an address generation stage operable to generate an address associated with an instruction for subsequent processing by said pipeline stages, said instruction being one from a first group of instructions or a second group of instructions, said address generation stage comprising:

address generation logic operable to receive operands associated with said instruction, to generate a shifted operand from one of said operands, and to add together, in dependence on said instruction, selected of said operands and said shifted operand to generate said address for subsequent processing by said pipeline stages; and

operand routing logic operable, in dependence on said instruction, to route operands associated with instructions from said first group of instructions to said address generation logic and to route operands associated with instructions from said second group of instructions via operand manipulation logic for manipulation of said operands prior to routing to said address generation logic.

2. The data processing apparatus of claim 1, wherein said instruction relates to a memory access and said address indicates a location in memory to be accessed.

3. The data processing apparatus of claim 1, wherein said first group of instructions comprises a first instruction which causes the processor core to logically add together two operands, and a second instruction which causes the processor core to logically add together one operand to another operand logically shifted by one of a predetermined number of bits.

4. The data processing apparatus of claim 3, wherein said address generation logic is operable to generate said another operand logically shifted by one of a predetermined number of bits.

5. The data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand to another operand logically shifted left by two bits.

6. The data processing apparatus of claim 5, wherein said address generation logic is operable to generate said another operand logically shifted left by two bits.

7. The data processing apparatus of claim 3, wherein said second instruction causes the processor core to logically add together one operand to another operand subject to only one preset logical shift operation.

8. The data processing apparatus of claim 1, wherein said address generation logic is operable to perform only one predetermined logical shift operation and operands associated with all other logical shift operations required by instructions from said second group of instructions are routed via operand manipulation logic for manipulation of operands prior to routing to said address generation logic.

9. The data processing apparatus of claim 3, wherein said second group of instructions comprises instructions which cause the processor core to logically add together one operand to another operand subject to any other logical shift operation.

10. The data processing apparatus of claim 9, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate said another operand logically shifted by any other number of bits.

11. The data processing apparatus of claim 1, wherein said second group of instructions comprises instructions which cause the processor core to logically subtract one operand from another operand.

12. The data processing apparatus of claim 11, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate an inverse representation of one of said operand and said another operand.

13. The data processing apparatus of claim 1, wherein said second group of instructions comprises a subtractive instruction for which said address is generated by subtracting a subtrahend operand from a minuend operand associated with said instruction, and said operand manipulation logic comprises subtraction operand generation logic operable to generate a negative representation of said subtrahend operand prior to routing to said address generation logic.

14. The data processing apparatus of claim 1, wherein said address generation logic comprises:

operand generation logic operable to receive a first operand associated with said instruction and to generate a shifted operand representative of said first operand shifted by a predetermined number of bits;

operand selection logic operable, in dependence on said instruction, to select one of said first operand and said shifted operand as a selected operand; and

addition logic operable to add a second operand associated with said instruction to said selected operand to generate said address for subsequent processing by said pipelined stages.

15. The data processing apparatus of claim 14, wherein said first operand comprises 'n'-bits, where 'n' is a positive integer, said operand generation logic receives said first operand over an 'n'-bit input bus and provides said shifted operand on an 'n'-bit output bus, said operand generation logic comprising:

interconnection logic operable to couple lines of the 'n'-bit input bus with lines of the 'n'-bit output bus to perform the shift operation.

16. The data processing apparatus of claim 14, wherein said operand selection logic is a two-input multiplexer.

17. The data processing apparatus of claim 14, wherein said operand selection logic is operable to select one of said first operand and said shifted operand as a selected operand in response to a selection signal generated by instruction decoder logic.

18. The data processing apparatus of claim 14, wherein said addition logic is a two-operand adder.

19. The data processing apparatus of claim 1, wherein said operand routing logic is operable to route operands in response to a routing signal generated by instruction decoder logic.

20. The data processing apparatus of claim 1, wherein said instruction is a subtraction instruction which causes the processor core to generate said address by subtracting a subtrahend operand in the form of an immediate from a minuend operand, and said data processing apparatus comprises instruction decoder logic operable to provide said subtrahend operand in negative form to said address generation stage and to generate a routing signal to cause said operand routing logic to route operands to said address generation logic.

21. The data processing apparatus of claim 1, wherein said instruction is one of a load instruction and a store instruction.

22. In a data processing apparatus comprising a processor core operable to process a sequence of instructions, said processor core having a plurality of pipeline stages, one of said plurality of pipeline stages being an address generation stage operable to generate an address associated with an instruction for subsequent processing by said pipeline stages, said instruction being one from a first group of instructions or a second group of instructions, a method of generating said address comprising the steps of:

a) receiving, at address generation logic, operands associated with said instruction;

b) generating a shifted operand from one of said operands;

c) adding together, in dependence on said instruction, selected of said operands and said shifted operand to generate said address for subsequent processing by said pipeline stages;

d) routing, in dependence on said instruction, operands associated with instructions from said first group of instructions to said address generation logic; and

e) routing, in dependence on said instruction, operands associated with instructions from said second group of instructions via operand manipulation logic for manipulation of said operands prior to routing to said address generation logic.

23. The method of claim 22, wherein said instruction relates to a memory access and said address indicates a location in memory to be accessed.

24. The method of claim 22, wherein said first group of instructions comprises a first instruction which causes the processor core to logically add together two operands, and a second instruction which causes the processor core to logically add together one operand to another operand logically shifted by one of a predetermined number of bits.

25. The method of claim 24, wherein said step (b) comprises generating said another operand logically shifted by one of a predetermined number of bits.

26. The method of claim 24, wherein said second instruction causes the processor core to logically add together one operand to another operand logically shifted left by two bits.

27. The method of claim 26, wherein said step (b) comprises generating said another operand logically shifted left by two bits.

28. The method of claim 24, wherein said second instruction causes the processor core to logically add together one operand to another operand subject to only one preset logical shift operation.

29. The method of claim 22, wherein said address generation logic is operable to perform only one predetermined logical shift operation.

30. The method of claim 24, wherein said second group of instructions comprise instructions which cause the processor core to logically add together one operand to another operand subject to any other logical shift operation.

31. The method of claim 30, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate said another operand logically shifted by any other number of bits.

32. The method of claim 22, wherein said second group of instructions comprises instructions which cause the processor core to logically subtract one operand from another operand.

33. The method of claim 32, wherein said operand manipulation logic is operable, in dependence on said instruction, to generate an inverse representation of one of said operand and said another operand.

34. The method of claim 22, wherein said second group of instructions comprises a subtractive instruction for which said address is generated by subtracting a subtrahend operand from a minuend operand associated with said instruction, and said operand manipulation logic comprises subtraction operand generation logic operable to generate a negative representation of said subtrahend operand prior to routing to said address generation logic.

35. The method of claim 1, wherein said step (a) comprises the step of receiving a first operand associated with said instruction, said step (b) comprises the step of generating a shifted operand representative of said first operand shifted by a predetermined number of bits and said step (c) comprises the steps of: selecting one of

said first operand and said shifted operand as a selected operand; and adding a second operand associated with said instruction to said selected operand to generate said address for subsequent processing by said pipelined stages.

36. The method of claim 35, wherein said first operand comprises 'n'-bits, where 'n' is a positive integer, said step (a) comprises receiving said first operand over an 'n'-bit input bus and said step (b) comprises providing said shifted operand on an 'n'-bit output bus by providing interconnection logic operable to couple lines of the 'n'-bit input bus with lines of the 'n'-bit output bus to perform the shift operation.

37. The method of claim 35, wherein said selecting step is performed by a two-input multiplexer.

38. The method of claim 35, wherein said selecting step comprises selecting one of said first operand and said shifted operand as a selected operand in response to a selection signal generated by instruction decoder logic.

39. The method of claim 35, wherein said addition step is performed by a two-operand adder.

40. The method of claim 22, wherein said steps (d) and (e) comprise routing operands in response to a routing signal generated by instruction decoder logic.

41. The method of claim 22, wherein said instruction is a subtraction instruction which causes the processor core to generate said address by subtracting a subtrahend operand in the form of an immediate from a minuend operand, and said data processing apparatus comprises instruction decoder logic operable to provide said subtrahend operand in negative form to said address generation stage and to generate a routing signal to cause said operands to be routed to said address generation logic.

42. The method of claim 22, wherein said instruction is one of a load instruction and a store instruction.